TUBF0306 Product Brief

1. Description

The TBUF0306 is an excellent clock buffer chip. It supports 1.5GHz frequency and 6 outputs with ultra-low delay and jitter. It is mainly used in applications such as low jitter, high-frequency clock / data distribution and level conversion.

The buffer can support input from 3 modes clock sources, such as single-ended clock or differential clock or crystal source.

The TBUF0306 can be allocated to two output groups A and B and one LVCMOS output.

Each channel output of A and B banks can be independently programmed to LVPECL, LVDS, HCSL or HIZ mode. The LVCMOS clock output is synchronized with the selected clock and can be enabled or disabled.

The TBUF0306 supports flexible voltage range. Both core voltage and IO voltage support 2.5V or 3.3V power supply.

2. Applications

- IT infrastructure (servers, storages)
- 5g communication
- Network system, including switches and routers
- ✧ Automotive electronics

3. Key Features

- Two inputs support including Single-Ended, Differential and Crystal
- 6 outputs support three modes including LVDS, LVPECL and HCSL
- Up to 1.5GHz Output Frequency for Differential Outputs
- Up to 200MHz Reference Output for LVCMOS
- Ultra-low Measured Jitter(typ<70fs Differential 100MHz)
- Low Delay from inputs to outputs channel(typ<0.8ns)
- Low Skew between outputs within different banks (typ<30ps)
- Flexible independent supply voltage of 3.3V/2.5V
- Lead-Free & Fully RoHS Compliant
- Industrial Temperature Support(-40℃~ 85℃)
- Environment-friendly without Halogen and Antimony
- 36-pin, 6mm x 6mm QFN package

4. Functional Diagram

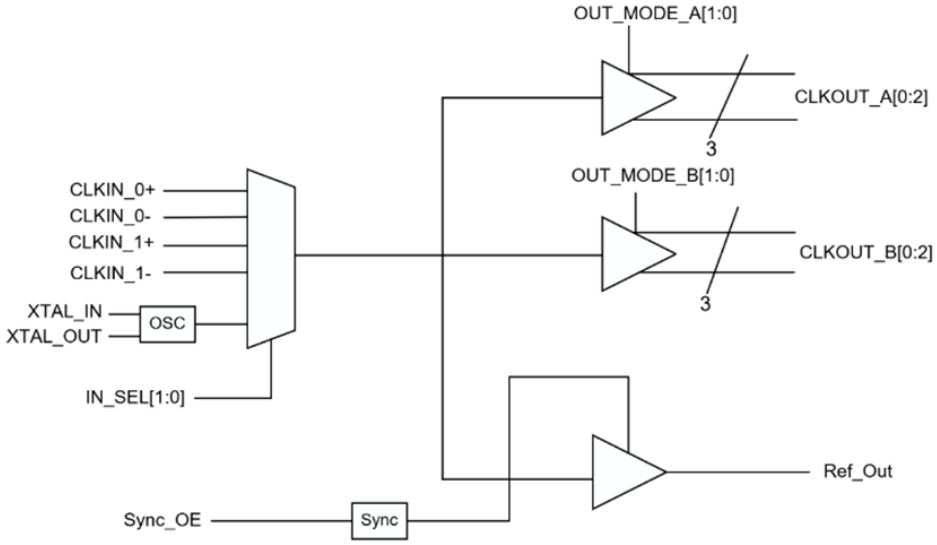

Figure 1 Functional Diagram

5. Pin Maps

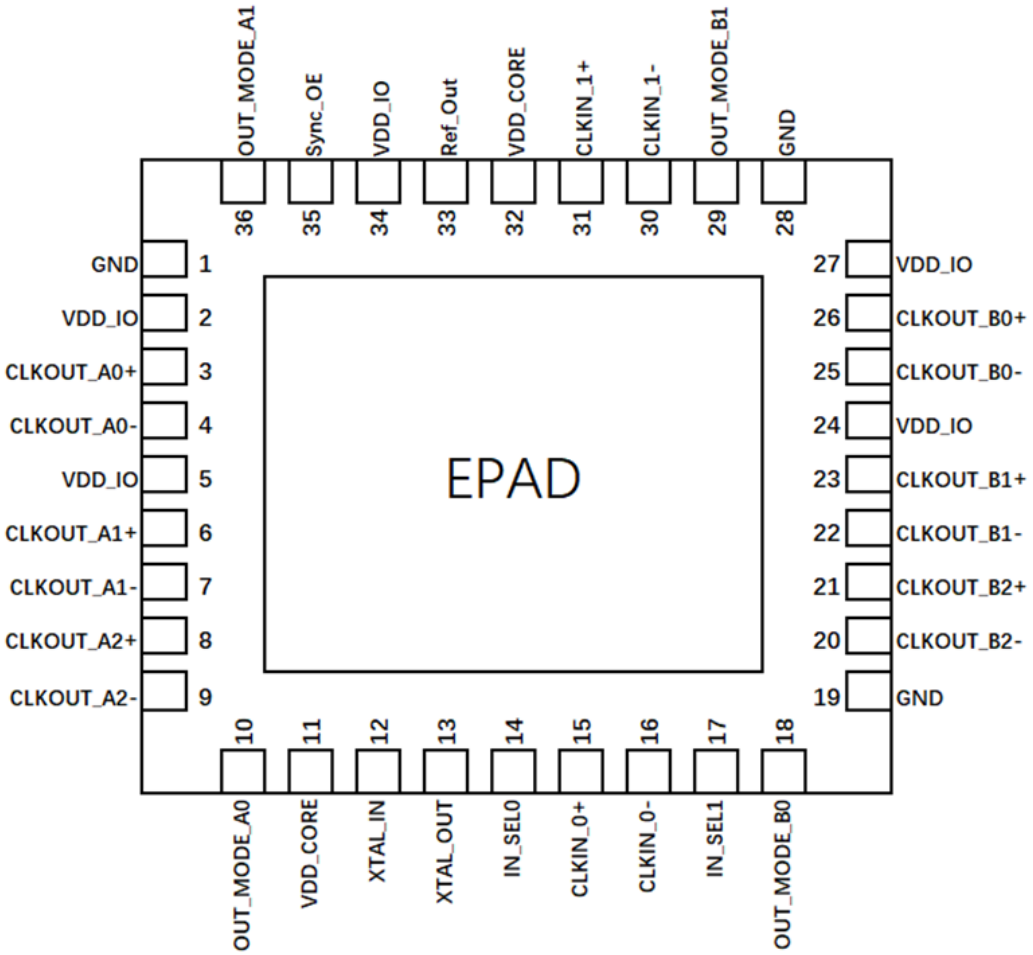

Figure 2 Pin Assignment Diagram-QFN36

6. Pin Descriptions

Table 1 Pin Descriptions

Pin #	Pin Name	Type	Description
3, 4	CLKOUT_A0+ CLKOUT_A0-	Output	Differential clock output P/N of BANK A Channel 0. Can be configured by OUT_MODE_A pins.
6, 7	CLKOUT_A1+ CLKOUT_A1-	Output	Differential clock output P/N of BANK A Channel 1. Can be configured by OUT_MODE_A pins
2, 5, 24, 27, 34	VDD_IO	Power	Power supply pins for Output buffers.
8, 9	CLKOUT_A2+ CLKOUT_A2-	Output	Differential clock output P/N of BANK A Channel 2. Can be configured by OUT_MODE_A pins
1, 19, 28	GND	Power	Ground pins.
10	OUT_MODE_A0	Input	Pulldown. Bank A output buffer type selection pins. View Table 3 for details.
36	OUT_MODE_A1	Input	
11, 32	VDD_CORE	Power	Power supply pins for core.
12	XTAL_IN	Input	Input pin for crystal supporting single ended input
13	XTAL_OUT	Output	Output pin for crystal. Leave XTAL_out OPEN if XTAL_in is driven by a single- ended clock.
14, 17	IN_SEL	Input	Pulldown. Clock input selections pins. View Table 2 for details.
15	CLKIN_0+	Input	Universal clock input 0, built_in deviation to 0.33VDD_CORE
16	CLKIN_0-	Input	Pullup/Pulldown. Reverse reference input 0, built_in deviation to 0.42VDD_CORE
18	OUT_MODE_B0	Input	Pulldown. Bank B output buffer type selection pins. View Table 2 for details.
29	OUT_MODE_B1	Input	
21, 20	CLKOUT_B2+ CLKOUT_B2-	Output	Differential clock output P/N of BANK B Channel 2. Can be configured by OUT_MODE_B pins.
23, 22	CLKOUT_B1+ CLKOUT_B1-	Output	Differential clock output P/N of BANK B Channel 1. Can be configured by OUT_MODE_B pins.
26, 25	CLKOUT_B0+ CLKOUT_B0-	Output	Differential clock output P/N of BANK B Channel 0. Can be configured by OUT_MODE_B pins.
30	CLKIN_1-	Input	Pullup/Pulldown. Reverse reference input 0, built_in deviation to 0.42VDD_CORE
31	CLKIN_1+	Input	Pulldown. Reverse reference input 0, built_in deviation to 0.33VDD_CORE
33	Ref_OUT	Output	Reference output, CMOS
35	Sync_OE	Input	Pulldown.Synchronous output supports Ref_Out. View Table 4 for details.
EPAD	EPAD	Gnd	Ground pins.