TGEN6310&10B&08&04&02 Product Brief

1. Description

The TGEN63xx series(TGEN6310/ TGEN6310B/ TGEN6308/ TGEN6304/ TGEN6302) are high-performance and low-jitter clock generator which integrates two any-frequency PLLs for applications that needs to meet PCIE specification or other scenarios. The ultra-low output clock jitter of TGEN63xx series clock generator provides more jitter margin in increasingly complex system, particularly HPC, Storage service, Data Center and Compute Server.

External Crystal(XTAL) or Crystal-Oscillator(XO) provides reference clock which is stable and low-jitter for built-in PLLS.The built-in PLLs can be configured or operate in integral multiplier or fractional multiplier mode independently, as well as Spread-Spectrum-Clock(SSC). Internal integral divider degrade the clock from PLL to a expected frequency, and deliver it to clock output driver. The TGEN63xx series support seven modes of outputs level described in corresponding section. Users can program TGEN63xx easily with GUI to generate any frequency. Factory preprogrammed are also available based on integrated NVM.

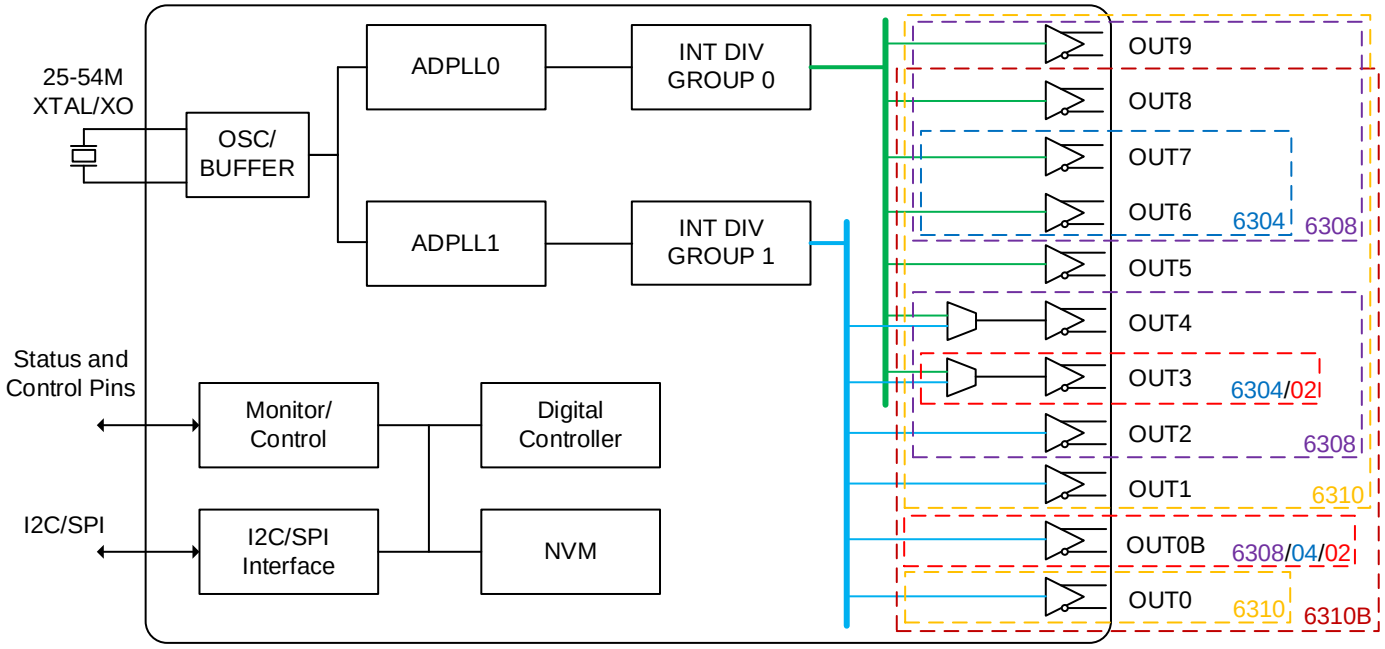
2. Applications

- Data Center
- X86 / Arm Server
- Automotive Electronics

3. Key Features

- PCIe Gen6 Common Clock(CC) 20fs RMS
- PCIe Gen5 Common Clock(CC) 80fs RMS
- Support PCIe CC/SRIS/SRNS clock architecture
- Highly Configurable Spread Spectrum Clock(SSC)
  - ✧ Modulation Depth: 0 - 5000ppm
  - ✧ Modulation Range: 30 - 33kHz
  - ✧ Spread Mode: Up or Down or Center Spread
- Reference Clock input frequency range
  - ✧ Crystal: 25 - 54MHz
  - ✧ Single-Ended and Differential: 10 - 100MHz
- Supported Output Mode
  - ✧ Single-Ended: LVCMOS
  - ✧ Differential: LVDS, LVPECL, CML, HCSL
- Output Clock frequency range
  - ✧ Single-Ended: 10 - 250MHz
  - ✧ Differential: 10 - 1200MHz(HCSL: 10 - 400MHz)
- Wide Power Supply range
  - ✧ VDD&VDDO: 1.8/2.5/3.3V
  - ✧ VDDA: 2.5/3.3V
  - ✧ Maximal Power Dissipation: 1.3W
- I2C and SPI Serial Interface supported(Maximal frequency for I2C: 400kHz, SPI: 20MHz)
- Support Factory or User Defined One-Time-Program(OTP) based on embedded NVM
- Lead-Free & Fully RoHS Compliant
- Industrial Temperature Support(-40°C~85°C)
- Environment-friendly without Halogen and Antimony
- Package information
  - ✧ TGEN6310/10B/08: 64-QFN 9x9mm package
  - ✧ TGEN6304/02: 44-QFN 7x7mm package

4. Functional Diagram



*All output channel name shown in this Figure is internal alias, not represent for particular model. See Section 4 for more and detailed information.

Figure 1 Functional Diagram

5. Pin Maps

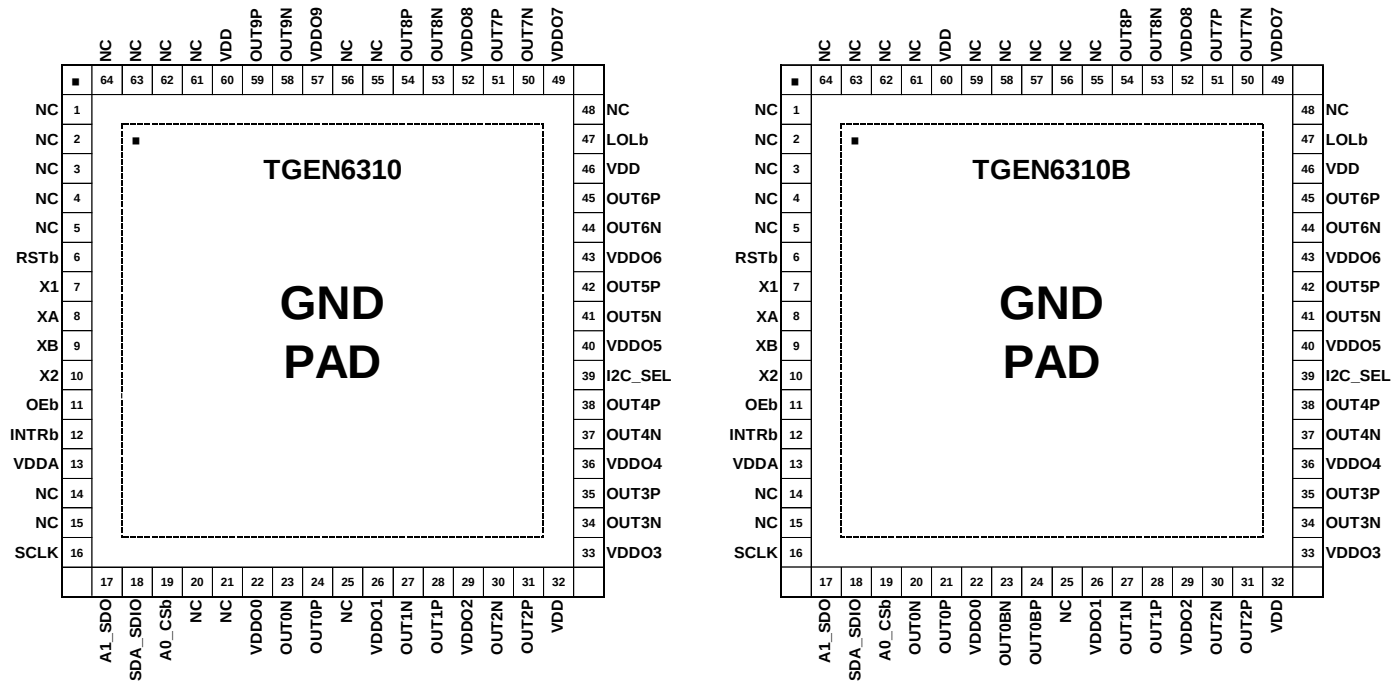


Figure 2 Pin Map of TGEN6310 and TGEN6310B

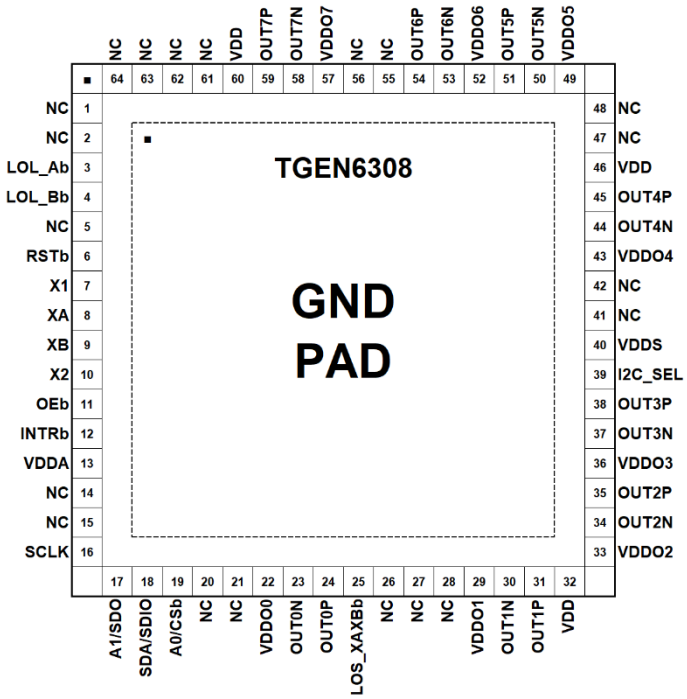


Figure 3 Pin Map of TGEN6308

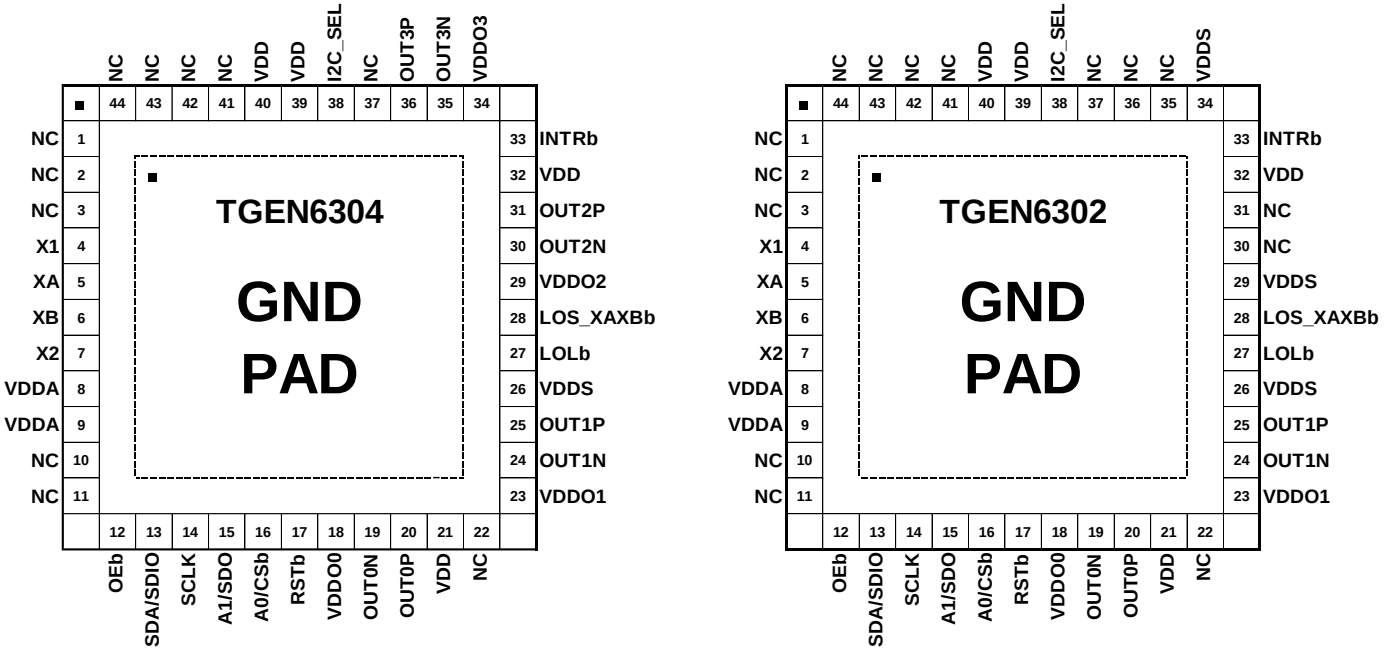


Figure 4 Pin Map of TGEN6304 and TGEN6302

6. Pin Descriptions

Table 1 64-QFN 9x9mm Pin List

Pin Name	Pin Number			Pin Type	Description
	TGEN 6310	TGEN 6310B	TGEN 6308		
Clock Input					
XA	8	8	8	I	Reference clock input pins. Connect to external crystal (XTAL) or external reference clock. XA have to connect a external reference clock when using a LVCMOS clock.
XB	9	9	9	I	
X1	7	7	7	I	External XTAL shield ground pins. Connect to XTAL GND directly. When routing PCB trace, the same net of X1, X2 and XTAL GND should be separated from GND plane of PCB. When using external reference clock, these two pins should be left disconnected and DO NOT connect to any net of the PCB.
X2	10	10	10	I	
Clock Output					
OUT0P	24	21	24	O	OUTxP/N are the clock out pins. Output mode, swing, common mode voltage, output impedance (only in LVCMOS mode) are configurable with corresponding register. If any output pin is not in use, it should be left unconnected.
OUT0N	23	20	23	O	
OUT0BP	-	24	-	O	
OUT0BN	-	23	-	O	
OUT1P	28	28	31	O	
OUT1N	27	27	30	O	
OUT2P	31	31	35	O	
OUT2N	30	30	34	O	
OUT3P	35	35	38	O	
OUT3N	34	34	37	O	
OUT4P	38	38	45	O	
OUT4N	37	37	44	O	
OUT5P	42	42	51	O	
OUT5N	41	41	50	O	
OUT6P	45	45	54	O	
OUT6N	44	44	53	O	
OUT7P	51	51	59	O	
OUT7N	50	50	58	O	
OUT8P	54	54	-	O	
OUT8N	53	53	-	O	
OUT9P	59	-	-	O	
OUT9N	58	-	-	O	
Serial Interface & Control & Status					
RSTb	6	6	6	I	Active low. When pulled low, a power-on reset signal will be sent to the device. All volatile memory will be set to the default state and no output is active. Once the external pull-down source is evacuated, the device will load the configuration from NVM(If it's programmed) and return to active state. This pin is pulled-up by a

Pin Name	Pin Number			Pin Type	Description
	TGEN 6310	TGEN 6310B	TGEN 6308		
					20 kΩ resistor internally and can be left unconnected when not in use.
OEb	11	11	11	I	Active low. When pulled low, all outputs are enable. This pin is pulled-up by a 20 kΩ resistor internally and can be left unconnected when not in use.
INTRb	12	12	12	O	Active low. When this pin is asserted low, at least one of the device status occurred. This pin should be left unconnected if not in use.
SCLK	16	16	16	I	This pin is the clock input pin for both I2C and SPI modes. When in I2C mode, this pin must be pulled-up to VDDA using a resistor of recommanedly 2.2kΩ. No pull-up resistor is required in SPI mode. Pull up or low when this pin is not in use.
SDA_SDIO	18	18	18	I/O	This is the bidirectional data pin (SDA) for the I2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when is SPI mode. Pull low when this pin is not in use.
A1_SDO	17	17	17	I/O	In I2C mode, this pin functions as the A1 address input pin and does not have an internal pull-up or pull-down resistor. In 4-wire SPI mode this is the serial data output (SDO) pin and drives high to the voltage of VDDA.
A0_CSb	19	19	19	I	This pin functions as the hardware controlled address A0 in I2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up by a ~20 kΩ resistor and can be left unconnected when not in use.
I2C_SEL	39	39	39	I	When pulled high, the device will use I2C as serial interface, and the address of I2C is determined by the level of pins A1_SDO and A0_CSb. When pulled low, the device will use SPI as serial interface. This pin is pulled-up by a 20 kΩ resistor internaly.
LOLb	47	47	-	O	Active low. When this pin is asserted low, at least one of the PLL is in state of Loss-Of-Lock. This pin should be left unconnected if not in use.
LOL_Ab	-	-	3	O	Active low. When this pin is asserted low, PLL0 is in state of Loss-Of-Lock. This pin should be left unconnected if not in use.
LOL_Bb	-	-	4	O	Active low. When this pin is asserted low, PLL1 is in state of Loss-Of-Lock. This pin should be left unconnected if not in use.
LOS_XAXBb	-	-	25	O	Active low. When this pin is asserted low, reference clock from XA/XB pins is lost. This pin should be left unconnected if not in use.
Power Supply					
VDD	32	32	32	P	Power supply for internal PLLs and dividers. This pin is an analog power supply pin and should be separated from digital power supply. A 1.0 µF and a 0.1 µF bypass capacitors should be placed very closed to each pin recommend.
	46	46	46	P	
	60	60	60	P	

Pin Name	Pin Number			Pin Type	Description
	TGEN 6310	TGEN 6310B	TGEN 6308		
VDDA	13	13	13	P	Power supply for analog module of reference clock input and internal logic. This pin is an analog power supply pin and should be separated from digital power supply. A 1.0 µF and a 0.1 µF bypass capacitors should be placed very closed to this pin recommend.
VDDO0	22	22	22	P	Power supply for OUTx outputs. Supply voltage in range of 3.3V, 2.5V, 1.8V is supported. Left power supply unconnected if the output is not in use to minimize power consumption.
VDDO1	26	26	29	P	
VDDO2	29	29	33	P	
VDDO3	33	33	36	P	
VDDO4	36	36	43	P	
VDDO5	40	40	49	P	
VDDO6	43	43	52	P	
VDDO7	49	49	57	P	
VDDO8	52	52	-	P	
VDDO9	57	-	-	P	
VDDS	-	-	40	P	Power supply for LOL_Ab and LOL_Bb outputs. Supply voltage in range of 3.3V, 2.5V, 1.8V is supported. A 1.0 µF and a 0.1 µF bypass capacitors should be placed very closed to this pin recommend.
GND	EPAD			G	Ground pin for TGEN63xx.
Not Used					
NC	1	1	1	-	TBD
	2	2	2	-	
	3	3	5	-	
	4	4	14	-	
	5	5	15	-	
	14	14	20	-	
	15	15	21	-	
	20	25	26	-	
	21	48	27	-	
	25	55	28	-	
	48	56	41	-	
	55	57	42	-	
	56	58	47	-	
	61	59	48	-	
	62	61	55	-	
	63	62	56	-	
	64	63	61	-	
	-	64	62	-	
	-	-	63	-	
	-	-	64	-	

Table 2 48-QFN 7x7mm Pin List

Pin Name	Pin Number		Pin Type	Describetion
	TGEN 6304	TGEN 6302		
Clock Input				
XA	5	5	I	Reference clock input pins. Connect to external crtstal(XTAL) or external reference clock. XA have to connect a external reference clock when using a LVCMOS clock.
XB	6	6	I	
X1	4	4	I	External XTAL sheld ground pins. Connect to XTAL GND directly. When routing PCB trace, the same net of X1, X2 and XTAL GND should be separated from GND plane of PCB. When using external reference clock, these two pins should be left disconnected and DO NOT connect to any net of the PCB.
X2	7	7	I	
Clock Output				
OUT0P	20	20	O	OUTxP/N are the clock out pins. Output mode, swing, common mode voltage, output impedence(only in LVCMOS mode) are configurable with corresponding register. If any output pin is not in use, it should be left unconnected.
OUT0N	19	19	O	
OUT1P	25	25	O	
OUT1N	24	24	O	
OUT2P	31	-	O	
OUT2N	30	-	O	
OUT3P	36	-	O	
OUT3N	35	-	O	
Serial Interface & Control & Status				
OEb	12	12	I	Active low. When pulled low, all outputs are enable. This pin is pulled-up by a 20 kΩ resistor internaly and can be left unconnected when not in use.
SCLK	14	14	I	This pin is the clock input pin for both I2C and SPI modes. When in I2C mode, this pin must be pulled-up to VDDA using a resistor of recommanedly 2.2kΩ. No pull-up resistor is required in SPI mode. Pull up or low when this pin is not in use.
SDA_SDIO	13	13	I/O	This is the bidirectional data pin (SDA) for the I2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when is SPI mode. Pull low when this pin is not in use.
A1_SDO	15	15	I/O	In I2C mode, this pin functions as the A1 address input pin and does not have an internal pull-up or pull-down resistor. In 4-wire SPI mode this is the serial data output (SDO) pin and drives high to the voltage of VDDA.
A0_CSb	16	16	I	This pin functions as the hardware controlled address A0 in I2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up by a ~20 kΩ resistor and can be left unconnected when not in use.
RSTb	17	17	I	Active low. When pulled low, a power-on reset signal will be sent to the device. All volatile memory will be set to the default state and no output is active. Once the external pull-down source is evacuated, the

Pin Name	Pin Number		Pin Type	Describetion
	TGEN 6304	TGEN 6302		
				device will load the configuration from NVM(If it's programmed) and return to active state. This pin is pulled-up by a 20 kΩ resistor internaly and can be left unconnected when not in use.
LOLb	27	27	O	Active low. When this pin is asserted low, at least one of the PLL is in state of Loss-Of-Lock. This pin should be left unconnected if not in use.
LOS_XAXBb	28	28	O	Active low. When this pin is asserted low, reference clock from XA/XB pins is lost. This pin should be left unconnected if not in use.
INTRb	33	33	I	Active low. When this pin is asserted low, at least one of the device status occured. This pin should be left unconnected if not in use.
I2C_SEL	38	38	I	When pulled high, the device will use I2C as serial interface, and the address of I2C is determined by the level of pins A1_SDO and A0_CSb. When pulled low, the device will use SPI as serial interface. This pin is pulled-up by a 20 kΩ resistor internaly.
Power Supply				
VDD	21	21	P	Pwer supply for internal PLLs and deviders. This pin is an analog power supply pin and should be separated from digital power supply. A 1.0 µF and a 0.1 µF bypass capacitors should be placed very closed to each pin recommendly.
	32	32	P	
	39	39	P	
	40	40	P	
VDDA	8	8	P	Power supply for analog module of reference clock input and internal logic. This pin is an analog power supply pin and should be separated from digital power supply. A 1.0 µF and a 0.1 µF bypass capacitors should be placed very closed to this pin recommendly.
	9	9	P	
VDDO0	18	18	P	Power supply for OUTx outputs. Supply voltage in range of 3.3V, 2.5V, 1.8V is supported. Left power supply unconnected if the output is not in use to minimize power consumption.
VDDO1	23	23	P	
VDDO2	29	-	P	
VDDO3	33	-	P	
VDDS	26	26	P	Power supply for LOL_Ab and LOL_Bb outputs. Supply voltage in range of 3.3V, 2.5V, 1.8V is supported. A 1.0 µF and a 0.1 µF bypass capacitors should be placed very closed to this pin recommendly.
	-	29	P	
	-	34	P	
GND	EPAD		G	Ground pin for TGEN63xx.
Not Used				
NC	1	1	-	TBD
	2	2	-	
	3	3	-	
	10	10	-	
	11	11	-	
	22	22	-	
	37	30	-	
	41	31	-	
	42	35	-	

Pin Name	Pin Number		Pin Type	Describetion
	TGEN 6304	TGEN 6302		
	43	36	-	
	44	37	-	
	-	41	-	
	-	42	-	
	-	43	-	
	-	44	-	