XUSB2104&2102 Product Brief

1. Overview

The XUSB2104/2102 are Universal Serial Bus 3.0 host controllers, which comply with Universal Serial Bus 3.0 Specification, and Intel's eXtensible Host Controller Interface(xHCI). These devices reduce power consumption and offer a smaller package footprint making them ideal for designers who wish to add the USB3.0 interface to mobile computing devices such as laptops and notebook computers.

The XUSB2104 supports four USB3.0 SuperSpeed ports and the XUSB2102 supports two USB3.0 SuperSpeed ports.

The XUSB2104/2102 use a PCI Express Gen 2 system interface bus allowing system designers to easily add up to four USB3.0 SuperSpeed ports to systems containing the PCI Express bus interface. When connected to USB 3.0 compliant peripherals, XUSB2104/2102 can transfer information at clock speeds of up to 5Gbps. The XUSB2104/2102 USB 3.0 standard are fully compliant and backward compatible with the previous USB2.0 standard. The new USB 3.0 standard supports data transfer speeds of up to ten times faster than those of the previous-generation USB2.0 standard, enabling quick and efficient transfers of large amounts of information.

2. Features

This chapter contains the following information:

- General
- PCIe
- USB Controller
- SPI Interface Controller

General

- 1.1V core and 3.3V I/O power supplies.
- Reference clock frequency of 24 MHz, generated by an external crystal.

PCIe

- PCIe 2.0 endpoint device.
- Compliant with PCIe 2.0 specifications.
- Supports communication at speed of 2.5 Gbps and 5 Gbps.
- Supports aggressive power management.
- Supports error reporting, recovery and correction.
- Supports Message Signaled Interrupt (MSI&MSI-X).
- Improved PCIe read request efficiency

USB Controller

- Compliant with Universal Serial Bus 3.0 Specification Revision 1.0, which is released by USB Implementers Forum, Inc
- Supports the following speed data rates: Low-Speed (1.5 Mbps) / Full-Speed (12 Mbps) / Hi-Speed (480 Mbps) / SuperSpeed (5 Gbps)
- Supports all USB compliant data transfer types as follows; Control / Bulk / Interrupt /Isochronous transfer
- Compliant with Intel's eXtensible Host Controller Interface (xHCI) Specification Revision 1.0
- Supports USB debugging capability on all SuperSpeed ports.
- Supports USB legacy function
- Supports USB Battery Charging Specification Revision 1.2 and other portable devices
    - DCP mode of BC 1.2
    - CDP mode of BC 1.2

- **SPI Interface Controller**
  - ✧ A four-pin SPI interface provides read and write access to an external SPI flash device for Firmware.
  - ✧ Supports Firmware Download Interface from system BIOS or system software
  - ✧ Vendor specific information stored in the external device is read by the controller during the chip power-up.

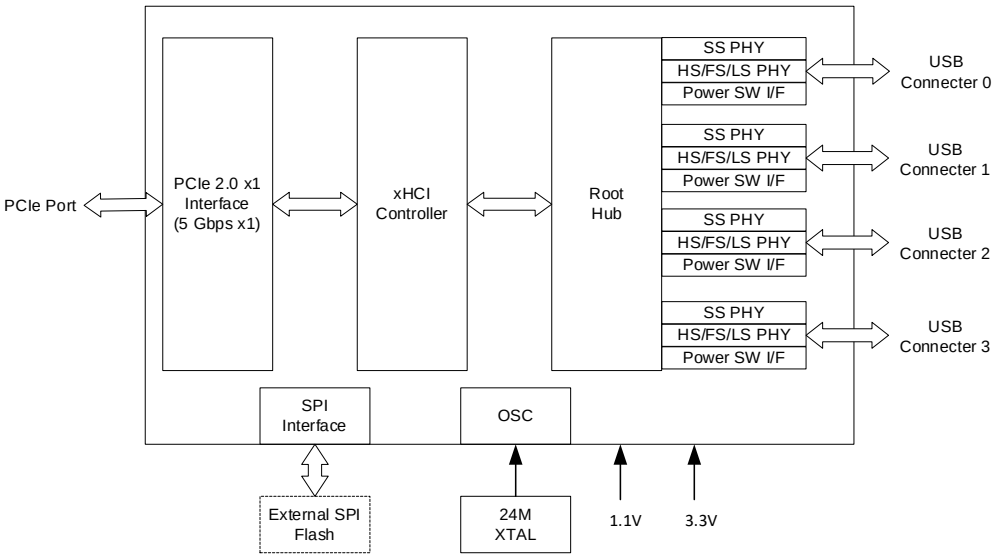

Figure 1 XUSB2104 Architecture

3. Pin Maps

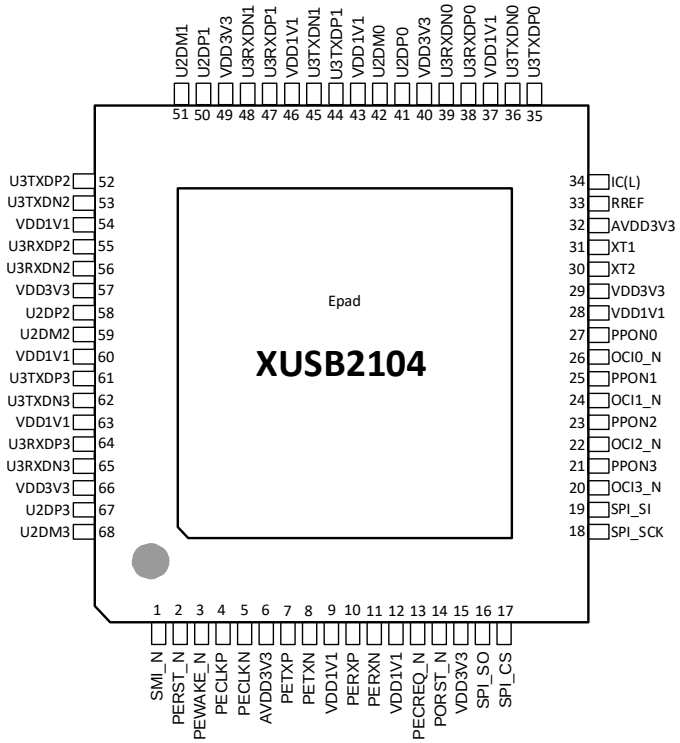

Figure 2 XUSB2104 Pin Assignment Diagram

The XUSB2104 68-pin LGA(compatible with QFN),pin diagram is illustrated in Figure 2.

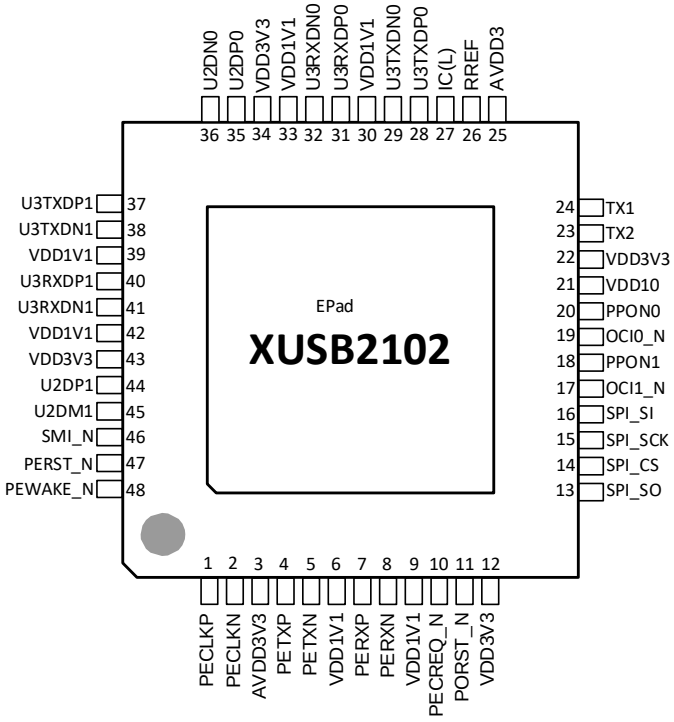

Figure 3 XUSB2102 Pin Assignment Diagram

The XUSB2102 48-pin LGA(compatible with QFN),pin diagram is illustrated in Figure 3.

4. Pin Descriptions

Signal Name	XUSB2104 Pin Number	XUSB2102 Pin Number	Description
PERST_N	2	47	PCI Express Platform Reset. Active low, indicates when the applied power is within the specified tolerance and stable.
WAKE_N	3	48	PCI Express Wake-Up. An open-drain, active low signal that is driven low by a PCIe function to reactivate the PCIe Link hierarchy's main power rails and reference clocks. Note: For applications that support a wake-up function, connect this pin to the WAKE# signal of a PCIe card slot or system board. Connect an external pull-up resistor from the PCIe card slot or system board to the 3.3V auxiliary supply. For applications that do not support a wake-up function, keep the WAKE_N pin on the XUSB2104/2102 open.
PECREQ_N	13	10	PCI Express "CLKREQ#" signal. This signal is used to request run/stop of reference clock.
CLKP	4	1	Reference Clock. Low voltage differential signals. The clock frequency has to be 100MHz.
CLKN	5	2	
PERXP	10	7	PCIe differential signals to the controller's receiver.

PERXN	11	8	
PETXP	7	4	PCIe differential signals from the controller's transmitter.
PETXN	8	5	
U3TXDP0	35	28	USB3.0 Transmit data D+ signal for SuperSpeed
U3TXDN0	36	29	USB3.0 Transmit data D- signal for SuperSpeed
U3RXDP0	38	31	USB3.0 Receive data D+ signal for SuperSpeed
U3RXDN0	39	32	USB3.0 Receive data D- signal for SuperSpeed
U2DP0	41	35	USB2.0 D+ signal for Hi-/Full-/Low-Speed
U2DM0	42	36	USB2.0 D- signal for Hi-/Full-/Low-Speed
OCI0_N	26	19	Over-current status input signal. 0: Over-current condition is detected 1: No over-current condition is detected
PPON0	27	20	USB port power supply control signal. 0: Power supply OFF 1: Power supply ON
U3TXDP1	44	37	USB3.0 Transmit data D+ signal for SuperSpeed
U3TXDN1	45	38	USB3.0 Transmit data D- signal for SuperSpeed
U3RXDP1	47	40	USB3.0 Receive data D+ signal for SuperSpeed
U3RXDN1	48	41	USB3.0 Receive data D- signal for SuperSpeed
U2DP1	50	44	USB2.0 D+ signal for Hi-/Full-/Low-Speed
U2DM1	51	45	USB2.0 D- signal for Hi-/Full-/Low-Speed
OCI1_N	24	17	Over-current status input signal. 0: Over-current condition is detected 1: No over-current condition is detected
PPON1	25	18	USB port power supply control signal. 0: Power supply OFF 1: Power supply ON
U3TXDP2	52	-	USB3.0 Transmit data D+ signal for SuperSpeed
U3TXDN2	53	-	USB3.0 Transmit data D- signal for SuperSpeed
U3RXDP2	55	-	USB3.0 Receive data D+ signal for SuperSpeed
U3RXDN2	56	-	USB3.0 Receive data D- signal for SuperSpeed
U2DP2	58	-	USB2.0 D+ signal for Hi-/Full-/Low-Speed
U2DM2	59	-	USB2.0 D- signal for Hi-/Full-/Low-Speed
OCI2_N	22	-	Over-current status input signal. 0: Over-current condition is detected 1: No over-current condition is detected
PPON2	23	-	USB port power supply control signal. 0: Power supply OFF 1: Power supply ON
U3TXDP3	61	-	USB3.0 Transmit data D+ signal for SuperSpeed
U3TXDN3	62	-	USB3.0 Transmit data D- signal for SuperSpeed
U3RXDP3	64	-	USB3.0 Receive data D+ signal for SuperSpeed
U3RXDN3	65	-	USB3.0 Receive data D- signal for SuperSpeed
U2DP3	67	-	USB2.0 D+ signal for Hi-/Full-/Low-Speed
U2DM3	68	-	USB2.0 D- signal for Hi-/Full-/Low-Speed
OCI3_N	20	-	Over-current status input signal.

			0: Over-current condition is detected 1: No over-current condition is detected
PPON3	21	-	USB port power supply control signal. 0: Power supply OFF 1: Power supply ON
RREF	33	26	Reference resistor connection. This pin has to be connected to an external 200ohm 1% resistor to Ground
XT1	31	24	Oscillator in Connect to 24 MHz crystal.
XT2	30	23	Oscillator out Connect to 24 MHz crystal.
SPI_CLK	18	15	SPI Interface Clock.
SPI_SI	19	16	Serial Data Out. Connect to the serial flash device's serial data input (DI).
SPI_CS	17	14	SPI Interface Chip Select.
SPI_SO	16	13	Serial Data In. Connect to the serial flash device's serial data output (DO).
PORST_N	14	11	Power on reset signal. When supporting wakeup from D3cold, this signal should be pulled high with system auxiliary power supply.
SMI_N	1	46	System management Interrupt signal. This is controlled with the USB Legacy Support Control/Status register.
VDD3V3	15,29,40,49, 57,66	12,22,34,43	+3.3 V power supply
VDD1V1	9, 12, 28, 37, 43, 46, 54, 60, 63	6, 9, 21, 30, 33,39, 42	+1.1 V power supply
AVDD3V3	6,32	3,25	+3.3 V power supply for analog circuit.
GND	GND PAD	GND PAD	Connect to ground.
IC(L)	34	27	Test pin. Connect to ground.