TGEN6309 Product Brief

1. Description

The TGEN6309 is a high performance PCIe clock generator that provides nine 100MHz PCIe clocks from a 25 MHz crystal or external single-ended clock input. The clock outputs are compliant with PCIe Gen 1, Gen 2, Gen 3, Gen 3 SRNS, Gen 4, Gen 5, and Gen 6 Common Clock specifications. A spread spectrum control pin for EMI reduction is also available. The TGEN6309's small footprint and low power consumption make it an ideal clock solution for consumer and embedded applications.

2. PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

3. Typical Applications

- Data Center
- X86/Arm Server
- Multi-function printer
- Wireless access point

4. Key Specifications

- PCIe Gen6 CC Phase Jitter < 40fs rms
- PCI-Express Gen 1, Gen 2, Gen 3, Gen 4, Gen 5 and Gen6 Common Clock Compliant
- PCIe Gen5 CC Phase Jitter < 50fs rms
- PCIe Gen6 CC Phase Jitter < 40fs rms
- Gen 3 SRNS compliant
- Serial-ATA (SATA) support at 100 MHz

5. Key Features

- Low-power push-pull HCSL-compatible differential outputs
- No termination resistors required
- 25 MHz crystal input or external single-ended clock input
- Up to nine PCI-Express clock outputs
- I2C support with readback capabilities
- Supports 0%, -0.3% and -0.5% spread-spectrum amounts for EMI reduction
- Industrial temperature: -40 to 85°C
- 3.3V power supply
- 48-pin LGA package (Compatible with 48-pin QFN)

6. Output Features

- Three 25MHz output pairs
- Seven 100MHz output pairs with individual OE# pins
- Nine MXCLK output pairs multiplexable between 100MHz and 25MHz

7. Functional Diagram

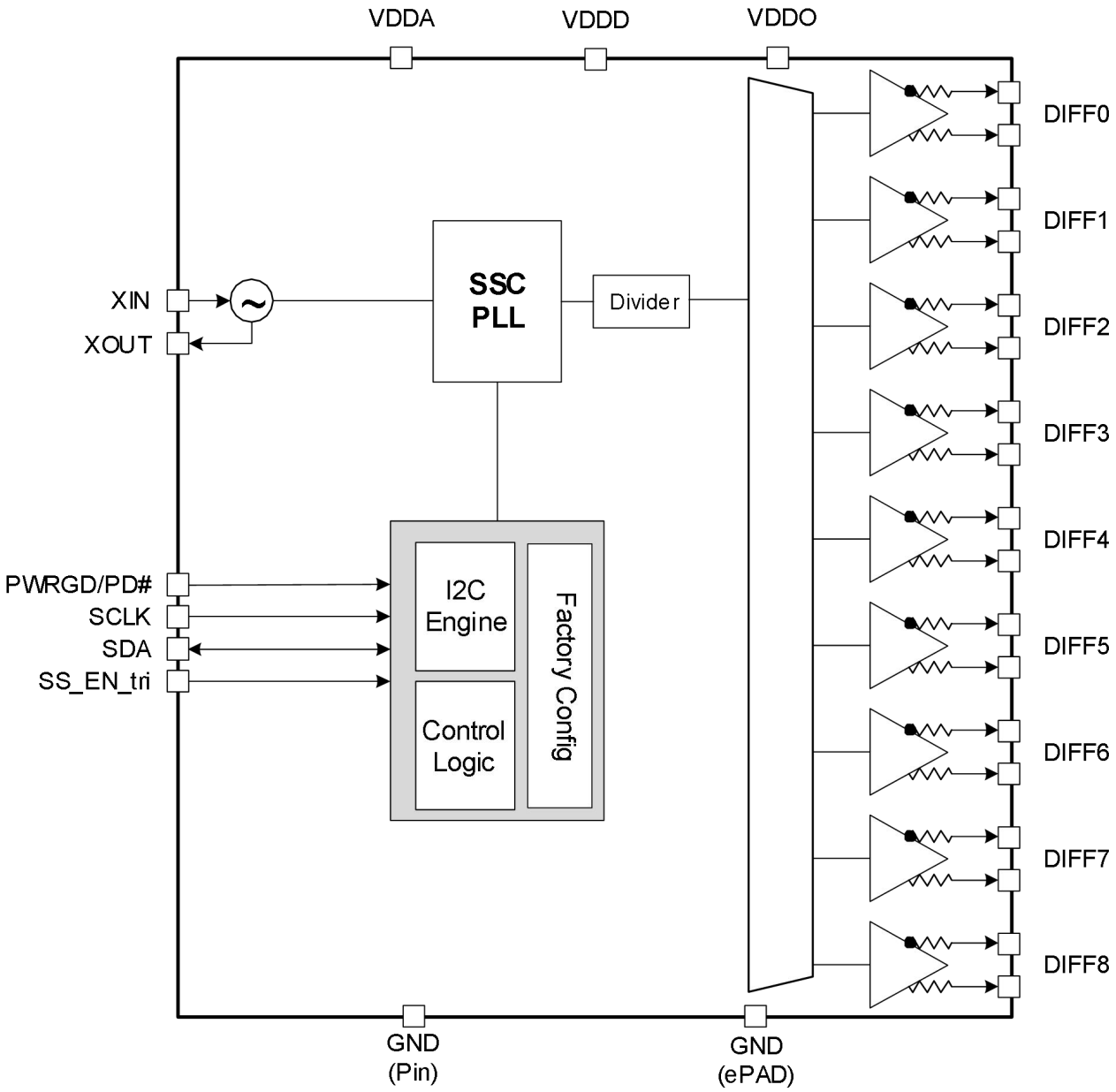

Figure 1 Functional Diagram

8. Pin Maps

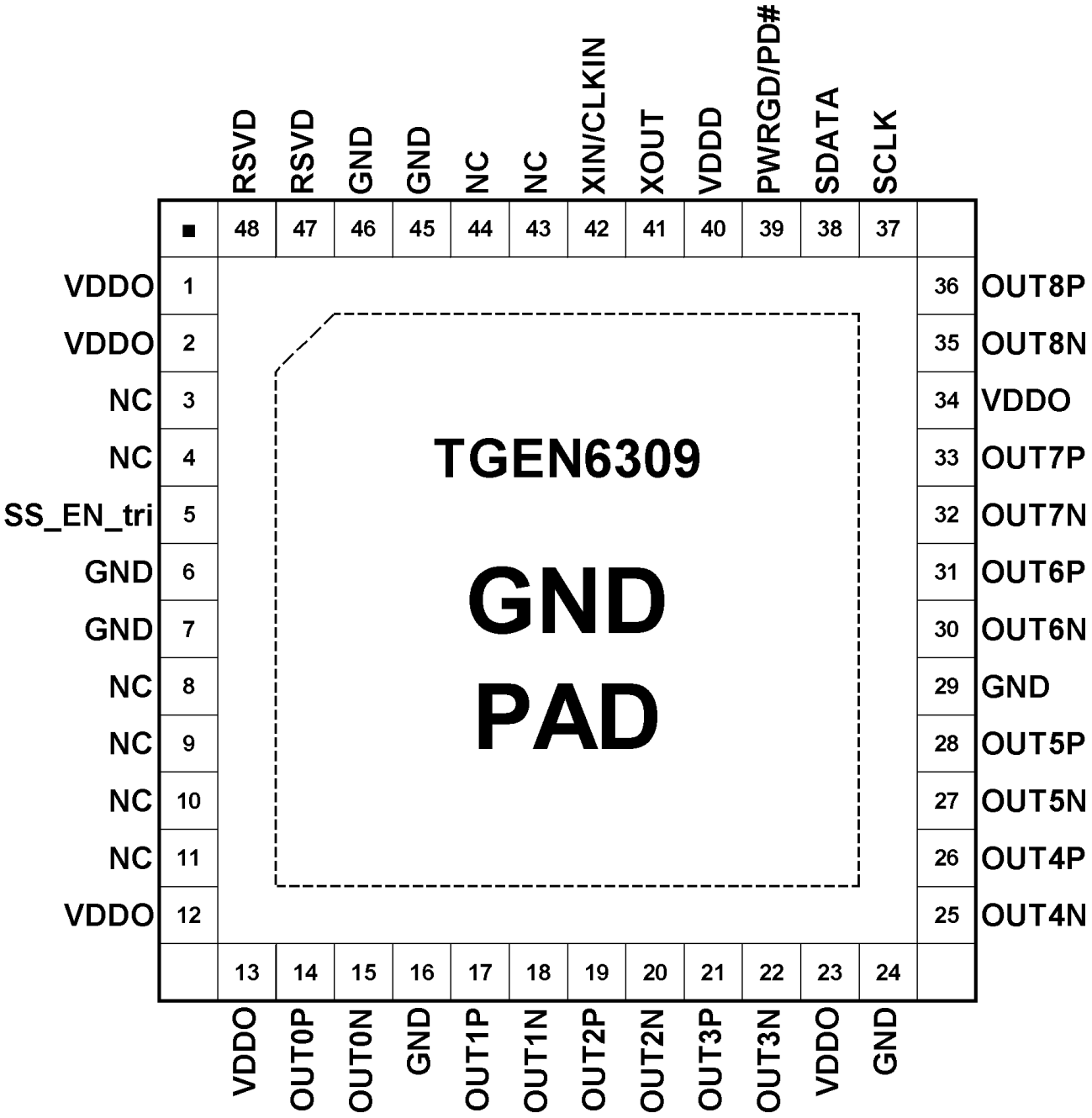

Figure 2 Pin Assignment Diagram-QFN100

9. Pin Descriptions

Table 1 Pin Descriptions

Number	Name	Type	Description
1	VDDO	PWR	Power supply for clock outputs.
2	VDDO	PWR	Power supply for clock outputs.
3	NC	-	No internal connection
4	NC	-	No internal connection
5	SS_EN_tri	I, PD, Z	Tri-level input to enable or disable spread spectrum. 0 = SSC off, MID = -0.3% max, and HIGH = -0.5% max.
6	GND	GND	Ground
7	GND	GND	Ground
8	NC	-	No internal connection
9	NC	-	No internal connection
10	NC	-	No internal connection
11	NC	-	No internal connection
12	VDDO	PWR	Power supply for clock outputs.
13	VDDO	PWR	Power supply for clock outputs.
14	OUT0P	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
15	OUT0N	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
16	GND	GND	Ground
17	OUT1P	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
18	OUT1N	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
19	OUT2P	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
20	OUT2N	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
21	OUT3P	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
22	OUT3N	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
23	VDDO	PWR	Power supply for clock outputs.
24	GND	GND	Ground
25	OUT4N	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
26	OUT4P	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
27	OUT5N	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
28	OUT5P	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
29	GND	GND	Ground
30	OUT6N	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
31	OUT6P	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
32	OUT7N	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
33	OUT7P	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
34	VDDO	PWR	Power supply for clock outputs.
35	OUT8N	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
36	OUT8P	O, DIF	±0.7V LP-HCSL differential 100MHz clock output.
37	SCLK	I	I2C compatible SCLK
38	SDATA	I/O	I2C compatible SDATA
39	PWRGD/PD#	I, PU	3.3V LVTTL input to power up(HIGH input) or power down(LOW input) the device.
40	VDDD	PWR	Power supply for internal digital module
41	XOUT	O	25.00 MHz crystal output, Float XOUT if using only CLKIN (Clock input).
42	XIN/CLKIN	I	25.00 MHz crystal input or 3.3 V, 25 MHz Clock Input.
43	NC	NC	No Connect
44	NC	NC	No Connect

Number	Name	Type	Description
45	GND	GND	Ground
46	GND	GND	Ground
47	RSVD	NC	Leave it unconnected, or connect to GND
48	RSVD	NC	Leave it unconnected, or connect to GND
EPAD	GND	GND	Ground for bottom pad of the IC