TGEN6320 Product Brief

1. Description

The TGEN6320 is a single-chip, PCIe Gen6 clock synthesizer. It is designed to work as a complete clock solution or in combination with DB2000Q-compliant clock buffers to provide point-to-point clocks to multiple receiving agents. It is part of the next generation clock generator family supporting the latest dual and multi-socket Intel server platforms.

2. PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

3. Typical Applications

- CK440Q

4. Key Specifications

- PCIe Gen6 CC Phase Jitter < 40fs rms

5. Key Features

- 3.3V operation
- Side-Band Interface allows real-time hardware control of all output enables
- OE# pin control of 100M[6:0] supports PCIe slot CLKREQ#
- 85Ω differential Low-Power HCSL (LP-HCSL) outputs eliminate 80 resistors, saving 130mm2 of area
- 9 selectable SMBus addresses
- Supports 0%, -0.3% and -0.5% spread-spectrum amounts
- 8 × 8 mm dual-row QFN-100

6. Output Features

- Three 25MHz output pairs
- Seven 100MHz output pairs with individual OE# pins
- Nine MXCLK output pairs multiplexable between 100MHz and 25MHz

7. Functional Diagram

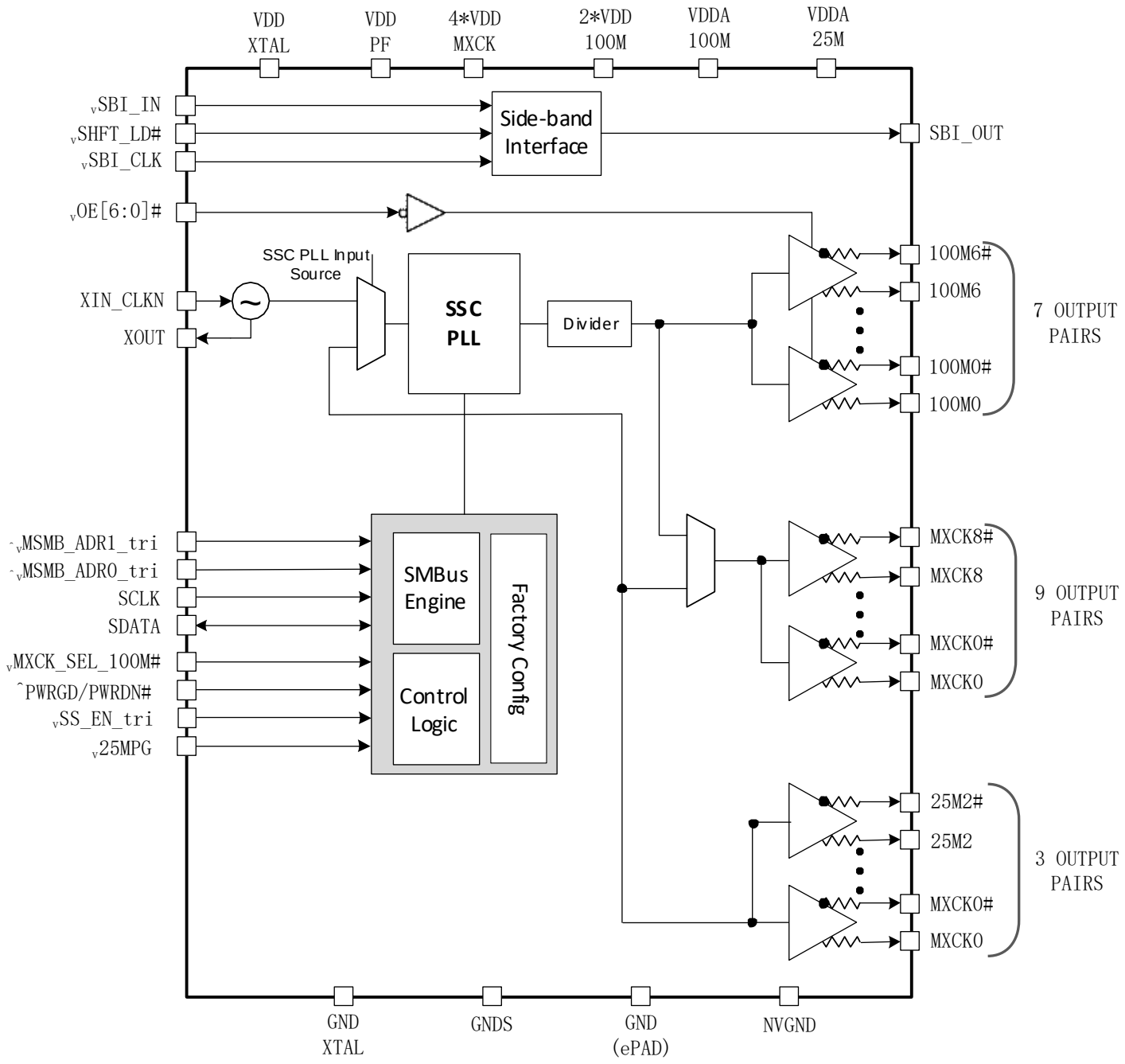

Figure 1 Functional Diagram

Note:

a) Pins with ^ prefix have internal pull-up resistor.

b) Pins with v prefix have internal pull-down resistor.

c) Pins with ^v prefix have internal

8. Pin Maps

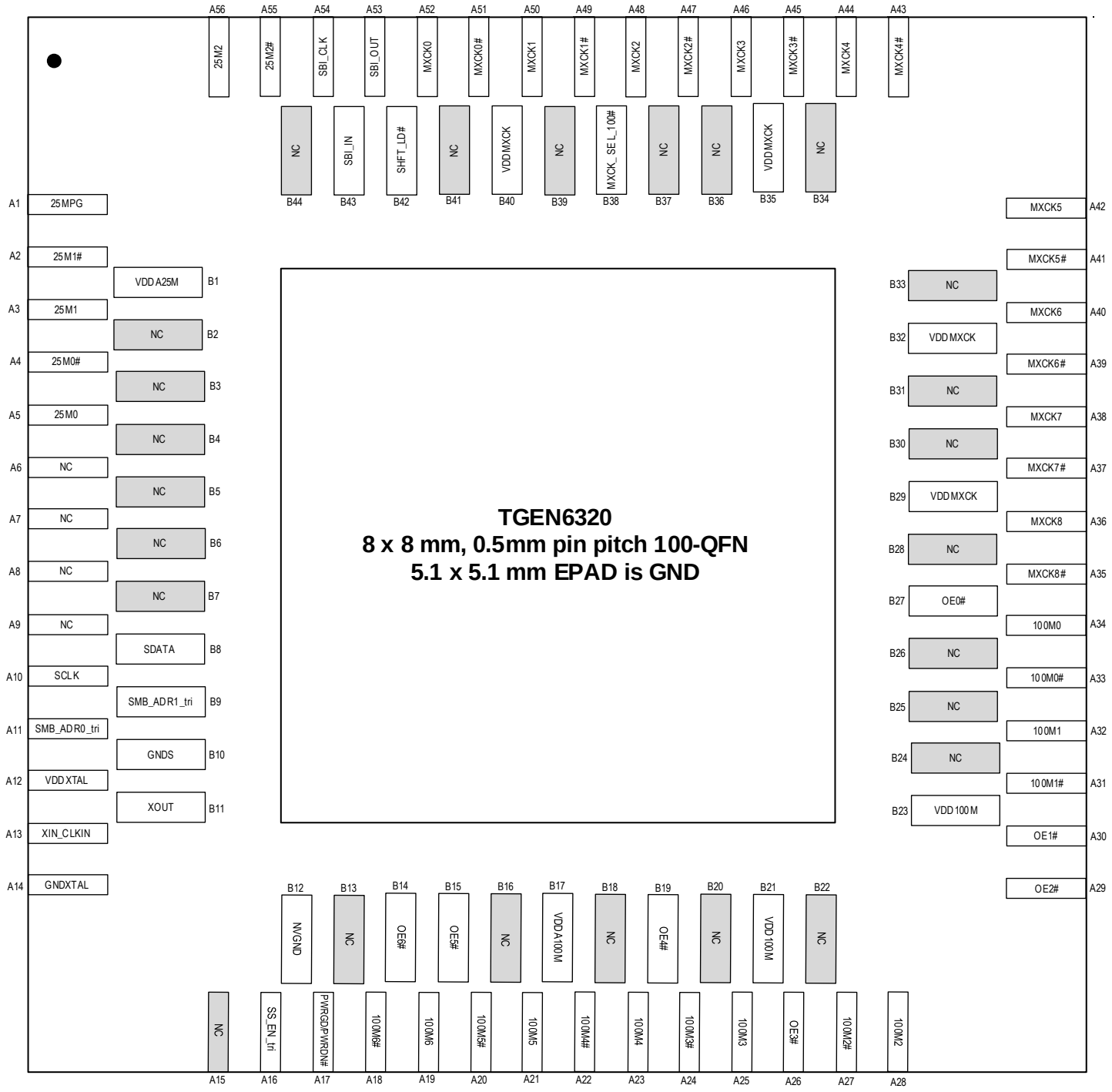

Figure 2 Pin Assignment Diagram-QFN100

9. Pin Descriptions

Table 1 Pin Descriptions

Number	Name	Type	Description
A34	100M0	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
A33	100M0#	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
A32	100M1	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
A31	100M1#	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
A28	100M2	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
A27	100M2#	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
A25	100M3	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
A24	100M3#	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
A23	100M4	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
A22	100M4#	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
A21	100M5	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
A20	100M5#	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
A19	100M6	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
A18	100M6#	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
A5	25M0	O, DIF	±0.7V LP-HCSL differential 25MHz true output.
A4	25M0#	O, DIF	±0.7V LP-HCSL differential 25MHz complement output.
A3	25M1	O, DIF	±0.7V LP-HCSL differential 25MHz true output.
A2	25M1#	O, DIF	±0.7V LP-HCSL differential 25MHz complement output.
A56	25M2	O, DIF	±0.7V LP-HCSL differential 25MHz true output.
A55	25M2#	O, DIF	±0.7V LP-HCSL differential 25MHz complement output.
A1	25MPG	I, SE, PDT, PD	3.3V LVTTL input to assert power good for the 25M2 output pair before PWRGD is asserted.
C1	EPAD	GND	Connect EPAD to ground.
B10	GNDS	GND	Package shield ground for crystal oscillator circuit. This pin is not connected internally.
A14	GNDXTAL	GND	GND for XTAL.
B38	MXCK_SEL_100M#	I, SE, PD	3.3V LVTTL input to select the source of the multiplexable clock outputs. 0 = 100 MHz, 1 = 25 MHz.
A52	MXCK0	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
A51	MXCK0#	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.
A50	MXCK1	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
A49	MXCK1#	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.
A48	MXCK2	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
A47	MXCK2#	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.
A46	MXCK3	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
A45	MXCK3#	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.