INTL9641 Product Brief

1. Description

The INTL9641 is a 2-to-1 I2C master demultiplexer with an arbiter function. It is designed for high reliability dual master I2C-bus applications where correct system operation is required, even when two I2C-bus masters issue their commands at the same time. The arbiter will select a winner and let it work uninterrupted, and the losing master will take control of the I2C-bus after the winner has finished. The arbiter also allows for queued requests where a master requests the downstream bus while the other master has control.

A race condition occurs when two masters try to access the downstream I2C-bus at almost the same time. The INTL9641 intelligently selects one winning master and the losing master gains control of the bus after the winning master gives up the bus or the reserve time has expired.

Multiple transactions can be done without interruption. The time needed for multiple transactions on the downstream bus can be reserved by programming the Reserve Time register. During the reserve time, the downstream bus cannot be lost.

Software reset allows a master to send a reset through the I2C-bus to put the INTL9641's registers into the power-on reset condition.

The Device ID of the INTL9641 can be read by the master and includes manufacturer,device type and revision.

When there is no activity on the downstream I2C-bus over 100 ms, optionally the INTL9641 will disconnect the downstream bus to both masters to avoid a lock-up on the I2C-bus.

The interrupt outputs are used to provide an indication of which master has control of the bus, and which master has lost the downstream bus. One interrupt input (INT_IN) collects downstream information and propagates it to the two upstream I2C-buses (INT0 and INT1) if enabled. INT0 and INT1 are also used to let the master know if the shared mail box has any new mail or if the outgoing mail has not been read by the other master. Those interrupts can be disabled and will not generate an interrupt if the masking option is set.

The pass gates of the switches are constructed such that the VDD pin can be used to limit the maximum high voltage, which will be passed by the INTL9641. This allows the use of different bus voltages on each pair, so that 1.8 V, 2.5 V, or 3.3 V devices can communicate with 3.3 V devices without any additional protection.

The INTL9641 does not isolate the capacitive loading on either side of the device, so the designer must take into account all trace and device capacitances on both sides of the device, and pull-up resistors must be used on all channels.

External pull-up resistors pull the bus to the desired voltage level for each channel. All I/O pins are 3.6 V tolerant.

An active LOW reset input allows the INTL9641A to be initialized. Pulling the RESET pin LOW resets the I2C-bus state machine and configures the device to its default state as does the internal Power-On Reset (POR) function

2. Applications

- High reliability systems with dual masters
- Gatekeeper multiplexer on long single bus
- Bus initialization/recovery for slave devices without hardware reset
- Allows masters without arbitration logic to share resources

3. Key Features

- 2-to-1 bidirectional master selector
- Channel selection via I2C-bus
- I2C-bus interface logic; compatible with SMBus standards
- 2 active LOW interrupt outputs to master controllers
- Active LOW reset input
- Software reset
- Four address pins allowing up to 112 different addresses
- Arbitration active when two masters try to take the downstream I2C-bus at the same time
- The winning master controls the downstream bus until it is done, as long as it is within the reserve time
- Bus time-out after 100 ms on an inactive downstream I2C-bus (optional)
- Readable device ID (manufacturer, device type, and revision)
- Bus initialization/recovery function
- Low Ron switches
- Allows voltage level translation between 1.8 V, 2.3 V, 2.5 V, 3.3 V and 3.6 V buses
- No glitch on power-up
- Supports hot insertion
- Software identical for both masters
- Operating power supply voltage range of 2.3 V to 3.6 V
- All I/O pins are 3.6 V tolerant
- Up to 1 MHz clock frequency
- ESD protection exceeds 6000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP16

4. Functional Diagram

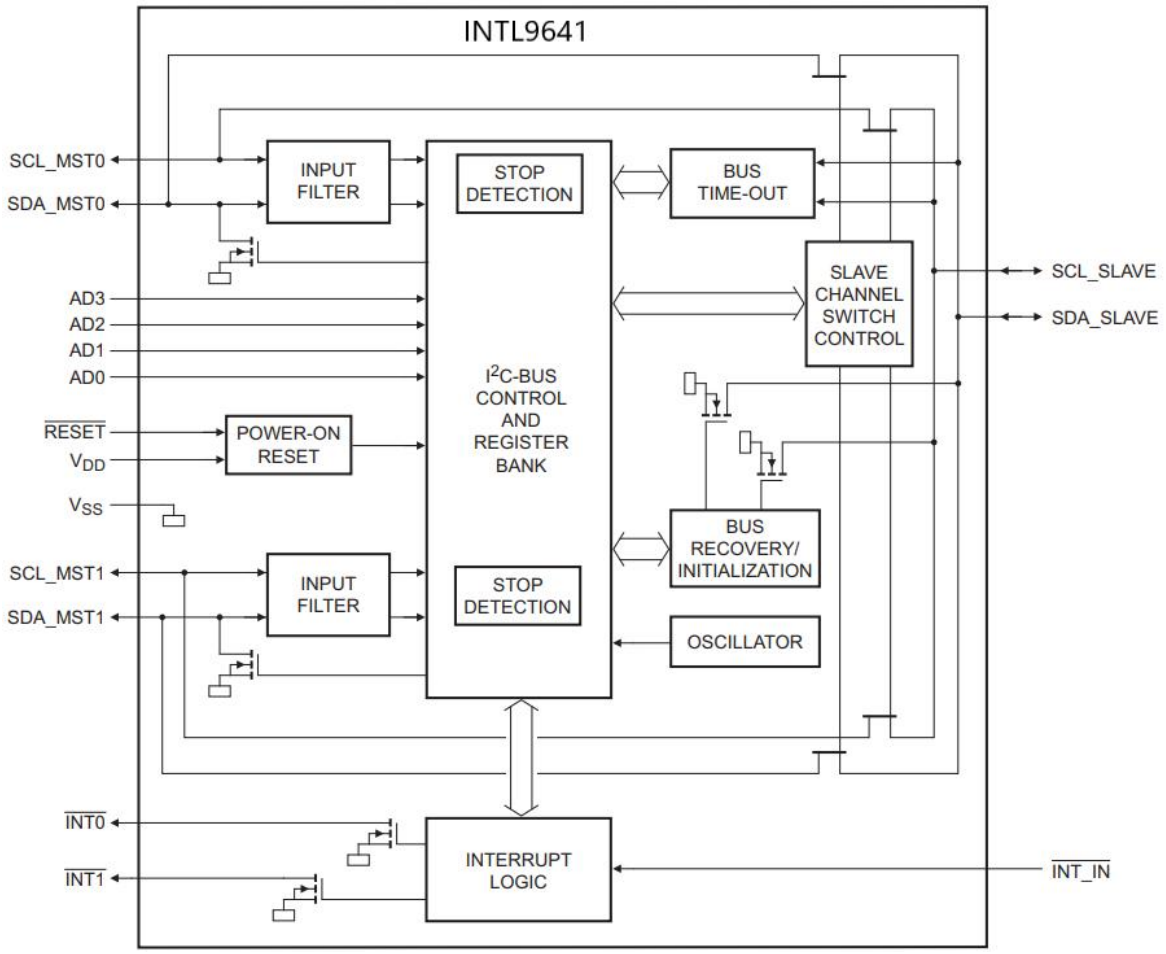

Figure 1 Block diagram of INTL9641

5. Pin Maps

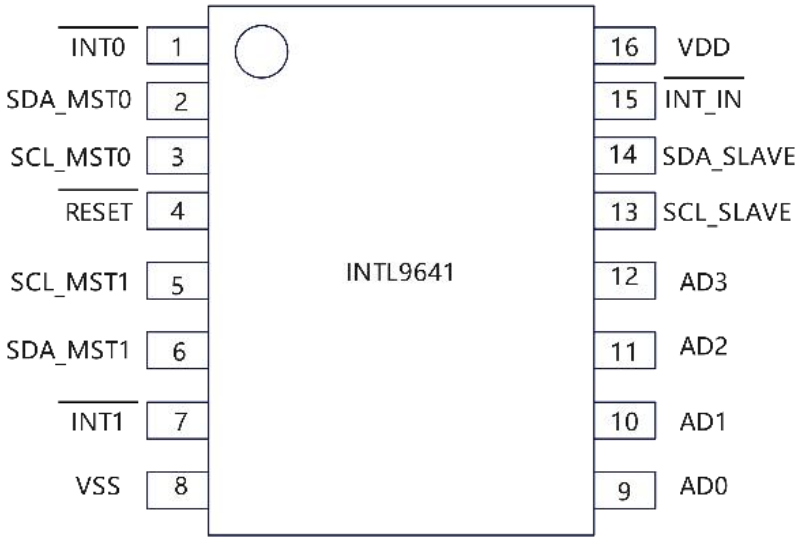

Figure 2 TSSOP16– Top View

6. Pin Descriptions

Table 1 Pin Descriptions

Symbol	Pin	Description
$\overline{INT0}$	1	active LOW interrupt output 0 (external pull-up required)
SDA_MST0	2	serial data master 0 (external pull-up required)
SCL_MST0	3	serial clock master 0 (external pull-up required)
$\overline{RESET}$	4	active LOW reset input (external pull-up required)
SCL_MST1	5	serial clock master 1 (external pull-up required)
SDA_MST1	6	serial data master 1 (external pull-up required)
$\overline{INT1}$	7	active LOW interrupt output 1 (external pull-up required)
GND	8	supply ground
AD0	9	address input 0 (externally held to GND, VDD, pull-up to VDD or pull-down to GND)
AD1	10	address input 1 (externally held to GND, VDD, pull-up to VDD or pull-down to GND)
AD2	11	address input 2 (externally held to GND, VDD, pull-up to VDD or pull-down to GND)
AD3	12	address input 3(externally held to GND, VDD, pull-up to VDD or pull-down to GND)
SCL_SLAVE	13	serial Clock slave (external pull-up required)
SDA_SLAVE	14	serial data slave (external pull-up required)
$\overline{INT\_IN}$	15	active LOW interrupt input (external pull-up required)
VDD	16	supply voltage